

REMARKS

In a final Office Action, claims 1, 3-5, 7-8 and 10-12 were examined. Claims 1 and 8 are amended. Claims 1, 3-5, 7-8 and 10-12 remain in the application.

The Patent Office rejects claims 1, 3-5, 7-8 and 10-12 under 35 U.S.C. §102(e). Reconsideration of the claims is requested in view of the above amendments and the following remarks.

The Patent Office rejects claims 1, 3-5, 7-8 and 10-12 under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,210,988 of Howe et al. (Howe).

Independent claim 1 describes a method comprising:

- (1) over an area of a substrate, forming a plurality of three dimensional first structures each including lateral side portions defining a distance from the surface of a substrate;
- (2) following forming the plurality of first structures, conformally introducing a sacrificial material over the area of the substrate including the lateral side portions of the plurality of first structures;
- (3) introducing a second structural material over the sacrificial material;
- (4) exposing a portion of the sacrificial material and a superior surface of the plurality of first structures, the superior surface opposing the surface of the substrate; and
- (5) removing the sacrificial material.

Howe does not disclose exposing a portion of a sacrificial material and a superior surface of the plurality of first structures. The Patent Office cites the MOSFET structures as corresponding to Applicants' first structures and SiO₂ as the sacrificial material. The Patent Office directs Applicants' attention to Figures 4 and 5 for a step of exposing a portion of the SiO₂. These figures, however, do not describe exposing a superior surface of the MOSFETs nor is there any description in the application that a superior surface of the MOSFETs are exposed.

Claims 3-5 and 7 depend from claim 1 and therefore contain all the limitations of claim 1. For at least the reasons stated with respect to claim 1, claims 3-5 and 7 are not anticipated by Howe.

Independent claim 8 describes a method comprising:

- (1) over an area of a surface of a substrate, lithographically patterning a plurality of first structures each including lateral side portions defining a distance from the surface of the substrate, the plurality of first structures having a first dimension about the surface of the substrate and a second different dimension;

(2) following forming the plurality of first structures, conformally introducing a sacrificial material layer over the area of the substrate including on the lateral side portions of the plurality of first structures;

(3) patterning the sacrificial material to expose a superior surface of the plurality of first structures, the superior surface opposing the surface of the substrate;

(4) forming second structures over the sacrificial material; and

(5) removing the sacrificial material.

Claim 8 is not anticipated by Howe, because Howe does not describe patterning a sacrificial material (e.g., SiO₂) to expose a superior surface of a plurality of first structures (MOSFETs).

Claims 10-12 depend from claim 8 and therefore contain all the limitations of claim 8. For at least the reasons stated with respect to claim 8, claims 10-12 are not anticipated by Howe.

Applicants respectfully request the Patent Office withdraw the rejection to claims 1, 3-5, 7-8 and 10-12 under 35 U.S.C. §102(e).

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance, and such action is earnestly solicited at the earliest possible date. If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nedy Calderon 12/15/04
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